PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-IPC/12/7448
Dated 18 Sep 2012

Voltage Reference, SOT23 Cu Wire Qualification in Carsem Malaysia

Table 1. Change Implementation Schedule

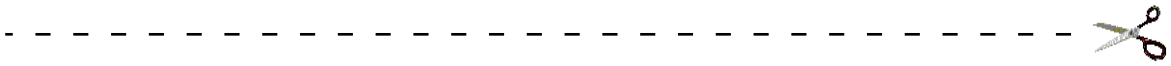
Forecasted implementation date for change	23-Nov-2012
Forecasted availability date of samples for customer	11-Sep-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	11-Sep-2012
Estimated date of changed product first shipment	18-Dec-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly material change
Reason for change	to improve service to ST Customers and standardize processes
Description of the change	Progressing on the activities related to quality improvement and along the plan of rationalizing the manufacturing processes, ST is glad to extend the implementation of CU Wire for the SOT23 package in the Carsem subcontractor (Malaysia). For the complete list of the part numbers affected by the change, please refer to the attached Products list. Samples of TS2431AILT and TS431AILT are available right now for immediate customer qual-ification, while the availability of other samples will be upon request.
Change Product Identification	QA number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPD-IPC/12/7448**
Please sign and return to STMicroelectronics Sales Office	**Dated 18 Sep 2012**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Riviera, Antonio	Marketing Manager
Naso, Lorenzo	Product Manager
Motta, Antonino	Q.A. Manager

WHAT:

Progressing on the activities related to quality improvement and along the plan of rationalizing the manufacturing processes, ST is glad to extend the implementation of CU Wire for the SOT23 package in the Carsem subcontractor (Malaysia).

For the complete list of the part numbers affected by the change, please refer to the attached Products list.
Samples of TS2431AILT and TS431AILT are available right now for immediate customer qualification, while the availability of other samples will be upon request.

WHY:
This manufacturing change will improve service to ST Customers, standardize processes for the affected package.

HOW:
The qualification program mainly consists of reliability tests and comparative electrical characterization.
The related reliability report is annexed to this document.
The changes here reported do not affect the electrical, dimensional and thermal parameters of the products, keeping unchanged all information reported on the relevant datasheets.

WHEN:

Te implementation will be finalized within Q3

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by the Q.A. number.

The changed here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change.
After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer’s written agreement.

Reliability Report

CARSEM MALAYSIA SOT23 3L CU WIRE QUALIFICATION

T.V.: TS2431AILT – Line: U782

General Information	
Product Line	U782
Product Description	Programmable shunt voltage reference
P/N	TS2431AILT
Product Group	IPD
Product division	Industrial & Power Conversion
Package	SOT23 3L
Silicon Process technology	BCD 2 - 2S

Locations	
Wafer fab	SINGAPORE Ang Mo Kio
Assembly plant	CARSEM M
Reliability Lab	IMS Catania Reliability Lab
Reliability assessment	Pass

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.1	26-Mar-2012	9	Stefania Motta	Giovanni Presti	FINAL

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Evaluation Process Change on SOT23 3L Cu wire qualification.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices be have correctly against environmental tests (no failure) until the final step @ 1000h. Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The TS2431 is a programmable shunt voltage reference with guaranteed temperature stability over the entire temperature range of operation -40 to +105°C. The output voltage may be set to any value between 2.5 and 24 V with an external resistor bridge.
Available in a SOT23-3 surface mount package, the device can be implemented in applications where space-saving is of utmost importance.

4.2 Construction note

	P/N TS2431AILT
Wafer/Die fab. information	
Wafer fab manufacturing location	Singapore Ang Mo Kio
Technology	BCD 2 - 2S
Process family	BCD2S
Die finishing back side	Lapped Silicon
Die size	1420, 760 micron
Bond pad metallization layers	2
Passivation type	P-Vapox(Sio2) / Nitride (Sin)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	ASL1K
Test program	TU782_1_0100.nx4
Assembly information	
Assembly site	Carsem M
Package description	SOT 23 3 LDS
Molding compound	Molding Compound Hitachi CEL82
Frame material	HDLF 3SOT23(438638) Copper AG
Die attach process	GLUE
Die attach material	QMI519 EPOXY
Die pad size	4X38MILS
Wire bonding process	Thermosonic
Wires bonding materials/diameters	1.0mil Cu wire
Final testing information	
Testing location	Carsem S
Tester	ASL1K
Test program	U782_2.nx4

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Package	Product Line	Comments
1	6133N2H	ENG14201	SOT 23 3L	U78201	I°lot AVG WB Parameters
2		ENG14204			2°lot AVG WB Parameters
3		ENG14205			3°lot AVG WB Parameters
4		ENG14202			High WB Parameters
5		ENG14203			Low WB Parameters

5.2 Test plan and results summary

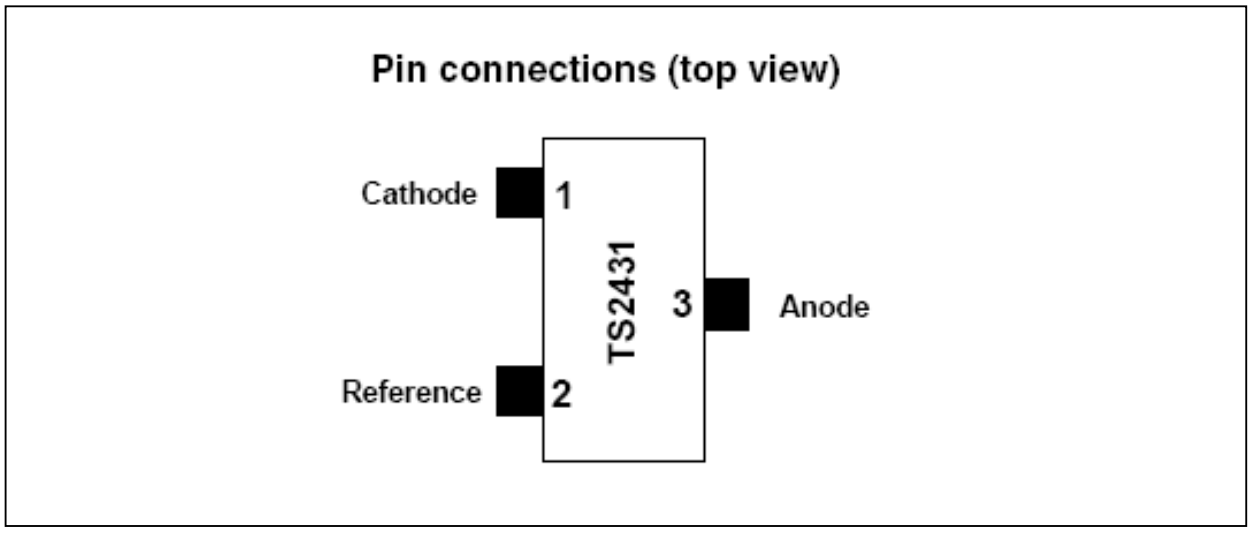
P/N TS2431AILT

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					note
						Lot 1 1°QUAL LOT	Lot 2 2°QUAL LOT	Lot 3 3°QUAL LOT	Lot 4 LOT HH	Lot 5 LOT LL	
Die Oriented Tests											
HTS	N	JESD22 A-103	Tj = 150℃	45	168 H	0/45	0/45	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	0/45	0/45	
HTOL	N	JESD22 A-108	Tj = 125℃, bias= +6.1V	77	168 H	0/77					
					500 H	0/77					
					1000 H	0/77					
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125℃ Store 168 H @ Ta=85℃ Rh=85% Oven Reflow @ Tpeak=260℃ 3 times	231	Final	Pass	Pass	Pass	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃	25	168 H	0/25	0/25	0/25	0/25	0/2 5	
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃	25	100 cy	0/25	0/25	0/25	0/25	0/25	
					300 cy	0/25	0/25	0/25	0/25	0/25	
					500 cy	0/25	0/25	0/25	0/25	0/25	
THB	Y	JESD22 A-101	Ta = 85℃, RH = 85%, bias= +5V	50	168 H	0/77					
					500 H	0/77					
					1000 H	0/77					

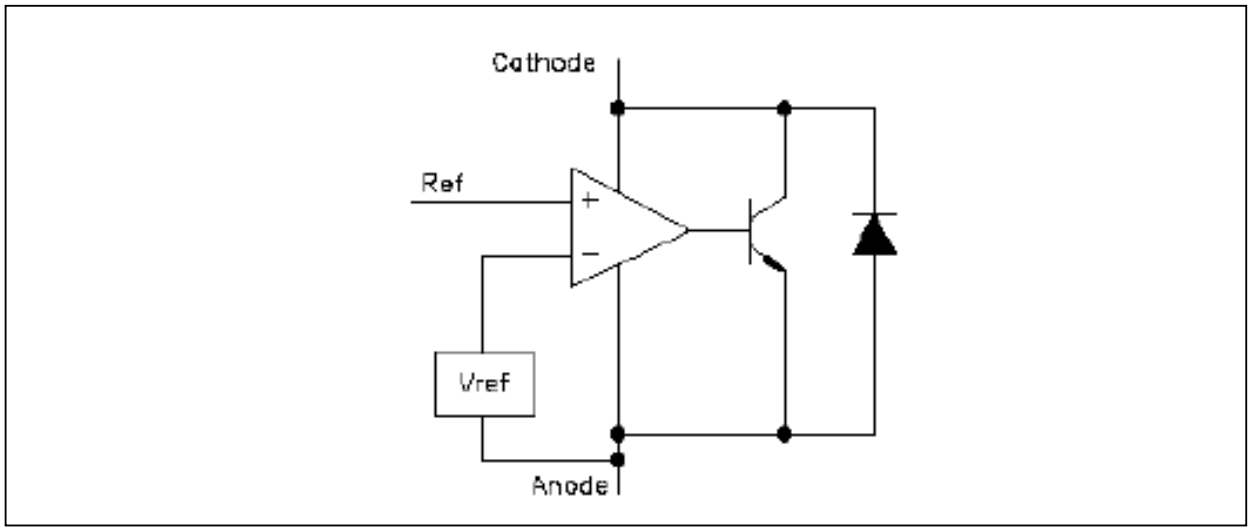
6 ANNEXES

6.1 Device details

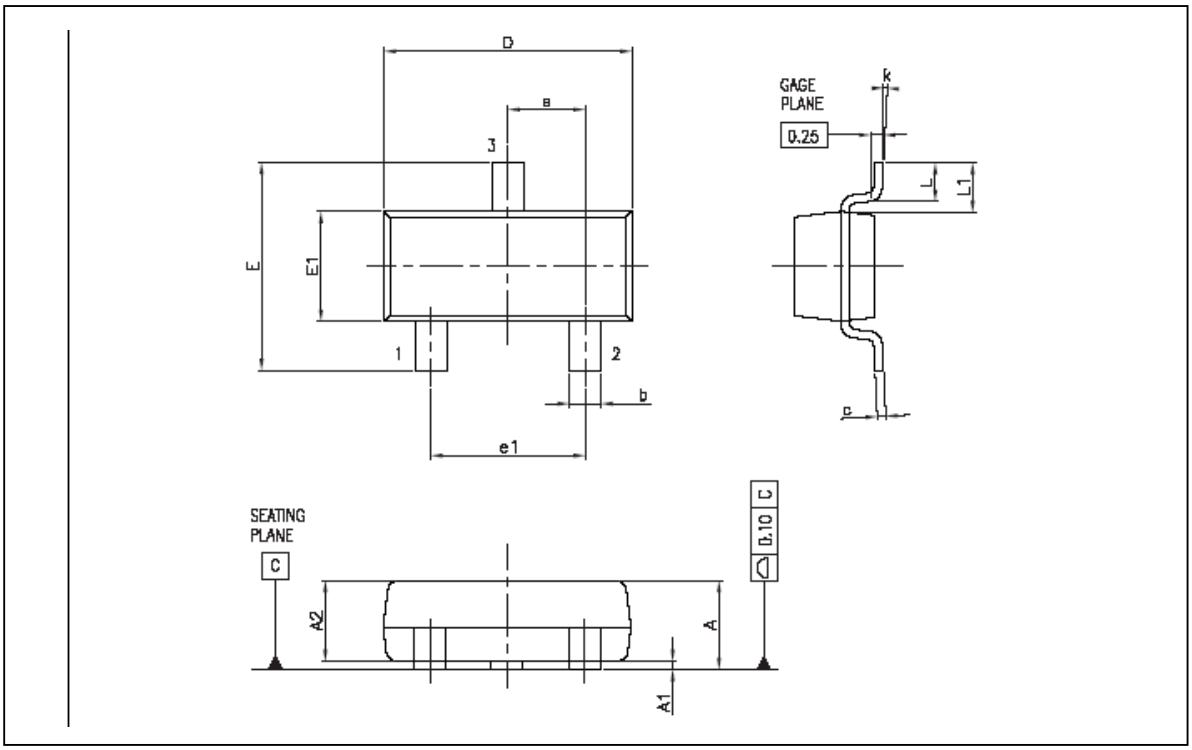
6.1.1 Pin connection



6.1.2 Block diagram



6.1.3 Package outline/Mechanical data



Dimensions						
Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.89		1.12	0.035		0.044
A1	0.01		0.10	0.0004		0.004
A2	0.88	0.95	1.02	0.035	0.037	0.040
b	0.30		0.50	0.012		0.020
c	0.08		0.20	0.003		0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10		2.64	0.083		0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e		0.95			0.037	
e1		1.90			0.075	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.54			0.021	
k	0d		8d			

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. Absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Reliability Report

Voltage References

CARSEM MALAYSIA SOT23 5L CU WIRE QUALIFICATION

T.V.: TS431AILT

Line S43101

Technology BICMOS 2

Packages: SOT23 5L

General Information	
Product Line	S43101
Product Description	LOW VOLTAGE ADJUSTABLE SHUNT REFERENCE
P/N	TS431AILT
Product Group	IPD
Product division	IND.& POWER CONV Linear Voltage Regulators & Vref
Packages	SOT23 5L
Silicon Process technology	BICMOS 2

Locations	
Wafer fab	*Ang Mo Kio*
Assembly plant	*Carsem*
Reliability Lab	*IMS Catania Reliability Lab*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	20 June 2012	8	Angelo Basile	Giovanni Presti	Final report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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2 GLOSSARY

SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Carsem Malaysia SOT23 5L Cu Wire Qualification

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure in the available steps). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation
The evaluation results are positive

3.3 Device description

The TS431 is a low-voltage, three-terminal, programmable shunt voltage reference. The output voltage can be set to any value between V_{ref} (1.24 V) and 6 V with two external resistors. The TS431 is able to operate at a lower voltage (1.24 V) and lower cathode current than the widely used TL431 and TL1431 shunt voltage reference. When driving an opt coupler, the TS431 is particularly useful for regulating 3.3 V switching power supplies

Construction note

	P/N
	TS431AILT SOT23 5
Wafer/Die fab. information	
Wafer fab manufacturing location	Carsem
Technology	BICMOS 2
Die finishing back side	Raw Silicon Back Grinding
Die size	900 x1350 um
Passivation type	P-Vapox(Sio2) / Nitride (Sin)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Singapore Ang Mo Kio
Tester	ASL1K
Test program	Vref_S431_0100.nx4
Assembly information	
Assembly site	Carsem
Package description	SOT 23-5
Molding compound	Hitachi CEL8240
Frame material	Copper Ag Spot (frame code 4
Die attach process	Glue
Die attach material	QMI519 EPOXY
Wire bonding process	Thermosonic Bonding
Wires bonding materials/diameters	1.0mil Cu wire
Lead finishing process	Electroplating
Lead finishing/bump solder material	100% Pure Matter Tin
Final testing information	
Testing location	Carsem
Tester	ASL1K
Test program	TS431_1.nx4

4 TESTS RESULTS SUMMARY

4.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Package	Product Line	Comments
1	61396X9	15205	SOT23 5L	S43101	1st Lot
2		15201			2nd Lot
3		15204			3rd Lot
4		15203			Corner Lot HH
5		15202			Corner Lot LL

4.2 Test plan and results summary

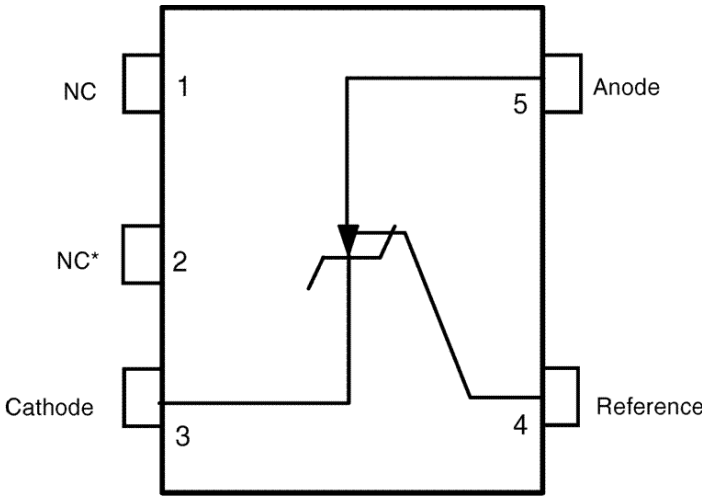
P/N TL431IDT

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				
						1st Lot	2nd Lot	3rd Lot	Corner Lot HH	Corner Lot LL
Die Oriented Tests										
HTOL	N	JESD22 A-108	Tj = 125℃, BIAS=+5V		168 H	0/77				
					500 H	0/77				
					1000 H	0/77				
HTSL	N	JESD22 A-103	Ta = 150℃		168 H	0/25	0/25	0/25	0/25	0/25
					500 H	0/25	0/25	0/25	0/25	0/25
					1000 H	0/25	0/25	0/25	0/25	0/25
Package Oriented Tests										
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121℃		96 H					
					168 H	0/25	0/25	0/25		
TC	Y	JESD22 A-104	Ta = -65℃ to 150℃		100 cy	0/25	0/25	0/25	0/25	0/25
					200 cy	0/25	0/25	0/25	0/25	0/25
					500 cy	0/25	0/25	0/25	0/25	0/25
THB	Y	JESD22 A-101	Ta = 85℃, RH=85%, BIAS =+3V		168 H	0/25	0/25	0/25		
					500 H	0/25	0/25	0/25		
					1000 H	0/25	0/25	0/25		
Other Tests										
ESD	N	AEC Q101-001, 002 and 005	HBM	3	+/- 2KV	PASS				
			MM	3	+/- 0.3KV	PASS				
			CDM	3	+/-500V all pins+/-750Vcorner pins	PASS				
WBP	N	MIL-STD-883-2011	Wire Bond Pull	10	Final	0/5	0/5			

5 ANNEXES

5.1 Device details

5.1.1 Pin connection

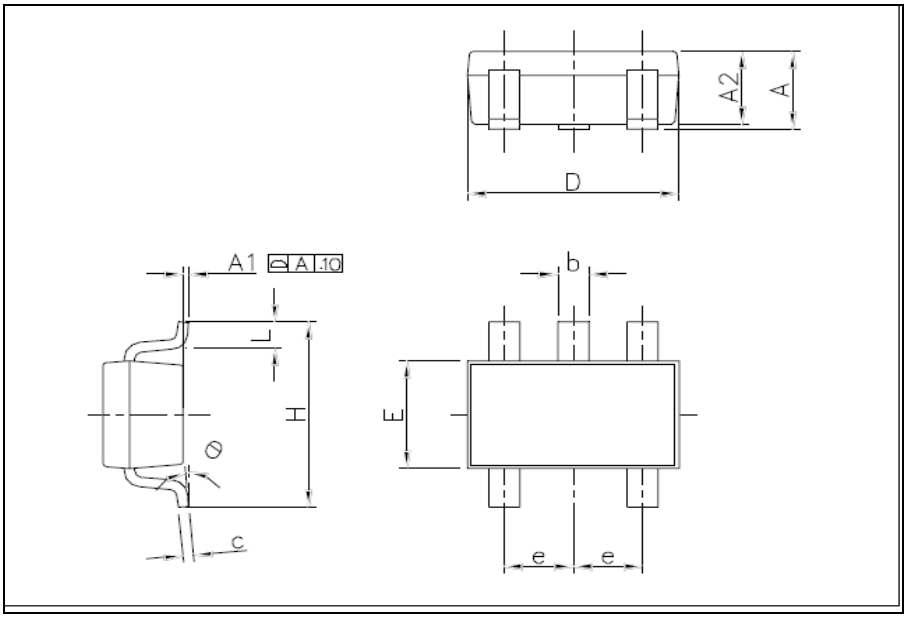


* Do not connect this pin or connect it to Anode

5.1.2 Package outline/Mechanical data

Table 4. SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0.00		0.15	0.00		0.006
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.014		0.02
C	0.09		0.20	0.003		0.008
D	2.80		3.00	0.110		0.118
H	2.60		3.00	0.102		0.118
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
e1		1.9			0.075	
L	0.35		0.55	0.014		0.022



5.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other Tests		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
WBP Wire Bond Pull	This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermo-compression, ultrasonic, or related techniques.	The purpose of this test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document.

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